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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/418,031	10/14/1999	SYUN-MING JANG	TSMC98-684/6	5530

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EXAMINER
VINH, LAN

ART UNIT	PAPER NUMBER
1765	17

DATE MAILED: 11/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/418,031	JANG ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- Th MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/1/2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. See attached PTO 948 form.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (US 6,312,874) in view of Huang et al (US 6,191,484)

Chan discloses a method for forming a dual damascene trench in a semiconductor substrate. This method comprises the steps of:

forming a substrate having a conductor/contact region 42 formed therein (col 4, lines 49-50)

forming a first lower layer 52 under a second upper layer 54 over the substrate (col 5, lines 11-14) which reads on forming over the substrate a first lower sub-layer and a second upper sub-layer. Chan also discloses that a subsequent etch step stops at the upper layer 54 (fig. 3a)

forming over the layer 52 and 54 an interlevel metal dielectric (IMD) layer 56 (silicon dioxide) (col 5, lines 16-17; fig.3b)

forming over the layer 56/IMD layer a patterned photoresist mask layer 62 having a pattern of an interconnection line trench pattern 64 centered over the contact layer 40 (col 5, lines 39-50; fig. 3b), etching using a first etching method to etch through layer 56/IMD layer and upper layer 54 to the first lower /sub-layer 52 (col 6, lines 1-4; fig. 3c)

etching the first lower layer 52 from the trench pattern using a second etch method (col 6, lines 7-9)

filling the trench pattern with conductive material 70 to form the damascene interconnection structure (col 6, lines 62-63)

Unlike the instant claimed invention as per claim 1, Chan does not specifically disclose using the first lower layer and second upper layer as a composite etch stop layer although Chan discloses using the second upper layer 54 as an etch stop layer.

However, Huang , in a method of forming multilevel metallization integrated circuit using etching, teaches that the etch stop layer may comprise a multiple layer/composite layer (col 4, lines 56-57)

Hence, one skilled in the art would have found it obvious to modify Chan method by using the first lower layer and second upper layer as a composite etch stop layer in view of Huang's teaching because Huang states that additional layer added to the single etch stop layer to form multiple-layers etch stop provides better etch stop control (col 4, lines 64-66)

Regarding claim 2, fig. 3c of Chan shows that the lower layer 52 prevents the etching of the conductor region

Regarding claim 3, Chan discloses using dry etch to selectively etch the layer 52 without etching the conductor region (col 6, lines 7-9) which reads on the layer 52 has a higher etch rate than the contact region.

Regarding claims 5-6, Chan's method of making a interconnect structure on a semiconductor substrate reads on forming a microelectronics semiconductor layer on a integrated circuit microelectronics fabrication.

4. Claims 4, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (US 6,312,874) in view of Huang et al (US 6,191,484) and further in view of Zhao et al (US 6,100,184)

Chan as modified by Huang has been described above in paragraph 3. Unlike the instant claimed invention as per claim 4, Chan and Huang do not disclose the step of forming a barrier metal layer over the patterned substrate.

However, Zhao discloses a method of making dual damascene comprises the step of forming a barrier metal layer 28 over the patterned substrate (col 8, lines 19-21)

Hence, one skilled in the art would have found it obvious to modify Chan and Huang by adding the step of a barrier metal layer 28 over the patterned substrate for the purpose of providing a barrier layer between the surrounding dielectric layer and the copper/conductor which will fill in the trench opening as taught by Zhao (col 8, lines 23-25)

Regarding claim 11, Chan discloses the conductor material is copper (col 4, lines 49-50)

5. Claims 7,10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (US 6,312,874) in view of Huang et al (US 6,191,484) and further in view of Zhao et al (US 6,245,663)

Chan as modified by Huang has been described above in paragraph 3. Unlike the instant claimed inventions as per claims 7, 10, Chan and Huang do not specifically disclose forming the lower dielectric layer (silicon oxide) and the IMD by PECVD and CVD.

However, Zhao, in a method for forming IC interconnect structure, teaches that silicon oxide/silicon dioxide material can be formed by PECVD and CVD (col 5, lines 50-60)

Hence, one skilled in the art would have found it obvious to modify Chan and Huang by forming the lower dielectric layer (silicon oxide) and the IMD by PECVD and CVD as per Zhao because Zhao teaches that it is known in the art that CVD process can be used to deposit stable oxide layers (col 5, lines 46-61)

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (US 6,312,874) in view of Huang et al (US 6,191,484) and further in view of Zhao et al (US 6,245,663)

Chan as modified by Huang has been described above in paragraph 3. Chan and Huang differ from the claimed invention as per claim 8 by forming a upper layer of silicon nitride instead of silicon oxynitride.

However, Zhao, in a method for forming IC interconnect structure, teaches that dielectric materials such as silicon nitride, silicon oxynitride can be formed by PECVD (col 5, lines 50-60)

Hence, one skilled in the art would have found it obvious to modify Chan and Huang by substituting the upper layer of silicon nitride with silicon oxynitride in view of Zhao's teaching because both materials are known dielectric material, thus the substitution of one for the other would have produced an expected result.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al (US 6,312,874) in view of Huang et al (US 6,191,484) and further in view of Ohashi et al (US 6,184,143)

Chan as modified by Huang has been described above in paragraph 3. Chan and Huang differ from the claimed invention as per claim 9 by forming a conductor region of copper instead of tungsten.

However, Ohashi, in a method for forming IC interconnect structure, teaches that tungsten can be used instead of copper for the main conductive layer (col 21, lines 31-32)

Hence, one skilled in the art would have found it obvious to modify Chan and Huang by substituting the copper in the conductive region with tungsten in view of Ohashi's teaching because both metals are known conductive material, thus the substitution of one for the other would have produced an expected result.

8. Claims 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao et al (US 6,100,184) in view of Huang et al (US 6,191,484) and further in view of Cronin et al (US 5,759,911)

Zhao discloses a method for making a dual damascene interconnect. This method comprises the steps of:

forming a substrate having a aluminum/metal conductive region (contact stud) 10 (col 4, lines 14-16)

forming over the substrate a lower dielectric organic polymer layer 14 (polyimide) and a upper dielectric etch stop layer 15 (col 6, lines 10-25 and fig. 3) reads on forming over the substrate a first lower organic polymer sub-layer and a second upper sub-layer

forming over the lower layer 14 and upper layer 15, an interlevel dielectric (ILD) layer 19 (silicon dioxide) (col 6, lines 61-65; fig. 11 shows that layer 19 is formed between layers 28 and 18)

forming over the IDL layer 19 a photoresist mask pattern 22 to define a subsequent via opening and trench opening centered over the contact region (col 7, lines 19-23 and fig. 7), utilizing a first plasma etching to etch through the ILD layer 19 and upper layer 15 to the lower polymer layer 14 (col 7, lines 25-34)

removing/stripping the photoresist mask and simultaneously etching the lower polymer layer 14 to complete the interconnection over the aluminum contact region (col 7, lines 30-45)

Unlike the instant claimed invention as per claim 12, Zhao does not specifically disclose using the first lower layer and second upper layer as a composite etch stop layer although Zhao discloses using the second upper layer 15 as an etch stop layer.

However, Huang , in a method of forming multilevel metallization integrated circuit using etching, teaches that the etch stop layer may comprise a multiple layer/composite layer (col 4, lines 56-57)

Hence, one skilled in the art would have found it obvious to modify Zhao method by using the first lower layer and second upper layer as a composite etch stop layer in view of Huang's teaching because Huang states that additional layer added to the single etch stop layer to form multiple-layers etch stop provides better etch stop control (col 4, lines 64-66)

Zhao and Huang also differ from the instant claimed invention as per claim 12 by using a contact region of aluminum instead of tungsten.

Cronin teaches that aluminum or tungsten can be used to fill contact region or stud connection in a semiconductor structure (col 10, lines 3-5)

Hence, one skilled in the art would also have found it obvious to substitute Zhao and Huang aluminum contact stud with tungsten stud in view of Cronin's teaching because aluminum and tungsten are known conductive material, thus the substitution of one for the other would have produced an expected result.

Regarding claim 13, fig. 8 of Zhao shows that the lower layer 14 prevents the etching of the conductor region 10.

Regarding claims 14, 20, Zhao discloses forming a barrier metal layer 28 (TaN) over the substrate and filling the trench with a conductor material to complete the interconnection structure (col 8, lines 35-40)

Regarding claim 16, Zhao discloses that lower polymer layer comprises of low dielectric constant spin-on-polymer such as polyimide (col 6, lines 15-17)

Regarding claim 17, Zhao discloses that upper layer 15 (silicon dioxide) is formed by CVD (col 6, lines 24-26)

Regarding claim 19, Zhao discloses filling the trench with aluminum or copper (col 8, lines 43-44)

Response to Arguments

9. Applicant's arguments with respect to the Hsiao reference have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 11/1/2002 with respect to the Zhao reference have been fully considered but they are not persuasive.

The applicants argue that layer 15 is not an ILD (interlevel dielectric layer) because Zhao teaches that layer 15 is an etch stop layer. This argument is not found persuasive because although the examiner recognizes that Zhao discloses that layer 15 is an etch stop layer, Zhao also discloses that layer 15 is a dielectric layer formed between two layer/level 14 and 18 (col 6, lines 36-37 and fig. 10). A dielectric layer formed between two layers/levels, as interpreted by the examiner, reads on an ILD

layer. Therefore, the examiner asserts that the Zhao reference reads on the claimed method.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin Utech can be reached on 703 308-3836. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9310 for regular communications and 703 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700

LV
November 8, 2002